What Is Claimed Is:

1. A method for producing a constant fullscale output in a delta-sigma analog-to-digital converter having a variable oversample ratio, the method comprising:

providing an analog delta-sigma modulator to generate a first digital signal from an analog input signal;

scaling the first digital signal according to the variable oversample ratio of the analog-to-digital converter to generate a second digital signal;

using the second digital signal as an input to a digital filter to generate a third digital signal; and

generating a digital output for the analog-to-digital converter from a portion of the third digital signal.

2. The method of claim 1, wherein having a variable oversample ratio comprises having a number of integer oversample ratios ranging from a minimum oversample ratio to a maximum oversample ratio.

3. The method of claim 1, wherein to generate a third digital signal comprises to generate a digital signal with a number of bits that is a function of the maximum oversample ratio of the analog-to-digital converter, the order of the digital filter, and the number of bits in the first digital signal.

4. The method of claim 1, wherein the digital filter is a comb filter.

5. The method of claim 4, wherein the comb filter comprises a cascade of integrators and differentiators.

6. The method of claim 5, wherein the number of integrators and differentiators is determined by the order of the digital filter.

7. The method of claim 5, wherein the integrators comprise the same number of bits as the third digital signal.

8. The method of claim 5, wherein the differentiators comprise the same number of bits as the digital output of the analog-to-digital converter.

9. The method of claim 1, wherein scaling the first digital signal according to the variable oversample ratio of the analog-to-digital converter to generate a second digital signal comprises using a decoder.

10. The method of claim 1, wherein scaling the first digital signal according to the variable oversample ratio of the analog-to-digital converter to generate a second digital signal comprises using a multiplier.

11. The method of claim 1, wherein the digital output for the analog-to-digital converter comprises a smaller number of bits than the third digital signal.

12. The method of claim 1, wherein generating a digital output for the analog-to-digital converter

comprises generating a fullscale digital output for a fullscale analog input.

13. A delta-sigma analog-to-digital converter circuit having a variable oversample ratio, the circuit comprising:

a delta-sigma analog modulator for generating a first digital signal from an analog input signal;

a digital circuit component for scaling the first digital signal according to the variable oversample ratio of the analog-to-digital converter to generate a second digital signal; and

a digital filter for generating a third digital signal from the second digital signal, wherein the third digital signal comprises a digital output for the analog-to-digital converter.

14. The circuit of claim 13, wherein the variable oversample ratio comprises a number of integer oversample ratios ranging from a minimum oversample ratio to a maximum oversample ratio.

15. The circuit of claim 13, wherein the digital circuit component comprises a decoder.

16. The circuit of claim 13, wherein the digital circuit component comprises a multiplier.

17. The circuit of claim 13, wherein the number of bits in the third digital signal is a function of the maximum oversample ratio of the analog-to-digital converter, the order of the digital filter, and the number of bits in the first digital signal.

18. The circuit of claim 13, wherein the digital filter is a comb filter.

19. The circuit of claim 18, wherein the comb filter comprises a cascade of integrators and differentiators.

20. The circuit of claim 19, wherein the number of integrators and differentiators is determined by the order of the digital filter.

21. The circuit of claim 19, wherein the integrators comprise the same number of bits as the third digital signal.

22. The circuit of claim 19, wherein the differentiators comprise the same number of bits as the digital output of the analog-to-digital converter.

23. The circuit of claim 13, wherein the digital output of the analog-to-digital converter comprises a smaller number of bits than the third digital signal.

24. The circuit of claim 13, wherein the digital output comprises a fullscale digital output for a fullscale analog input.

25. A method for reducing the die area, circuit complexity, and power dissipation in a delta-sigma analog-to-digital converter having a variable oversample ratio, the method comprising:

means for generating a first digital signal from an analog input;

means for scaling the first digital signal to produce a second digital signal; and

means for low-pass filtering the second digital signal to produce a third digital signal, wherein the third digital signal comprises a digital output for the analog-to-digital converter.

26. The method of claim 25, wherein the variable oversample ratio comprises a number of integer oversample ratios ranging from a minimum oversample ratio to a maximum oversample ratio.

27. The method of claim 25, wherein the means for generating a first digital signal from an analog input comprises a delta-sigma analog modulator.

28. The method of claim 25, wherein the means for scaling the first digital signal to produce a second digital signal comprises a decoder.

29. The method of claim 25, wherein the means for scaling the first digital signal to produce a second digital signal comprises a multiplier.

30. The method of claim 25, wherein the means for low-pass filtering the second digital signal to produce a third digital signal comprises a comb filter.

31. The method of claim 30, wherein the comb filter comprises a cascade of integrators and differentiators.

32. The method of claim 25, wherein the number of bits in the third digital signal is a function of the maximum oversample ratio of the analog-to-digital converter, the order of the digital filter, and the number of bits in the first digital signal.

33. The method of claim 32, wherein the number of integrators and differentiators is determined by the order of the digital filter.

34. The method of claim 31, wherein the integrators comprise the same number of bits as the third digital signal.

35. The method of claim 31, wherein the differentiators comprise the same number of bits as the digital output of the analog-to-digital converter.

36. The method of claim 25, wherein the digital output of the analog-to-digital converter comprises a smaller number of bits than the third digital signal.

37. The method of claim 25, wherein the digital output comprises a fullscale digital output for a fullscale analog input.